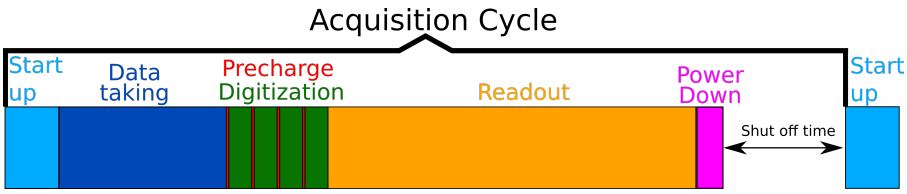

Figure 1: KPiX event time structure.

1 The KPiX readout

The KPiX readout chips is a silicon chips used in hybrid silicon detectors for readout some of its design parameters are:

- 13 bit ADC
- 1024 readout channels
- integrated pitch adapter
- Only active for a short time span and deactivated for the rest of the time thanks to power pulsing (see fig.: 1)
- Power consumption of $\approx 40\,\mu W$ per channel as a result of power pulsing
- TODO?

As a result of the power pulsing KPiX is only active for a short time span depending on the parameters. The actual data taking time is

$$T_{\text{Readout}} = 8 \times \text{ClkPeriodAcq} \times \text{BunchClockCount} \tag{1}$$

with an approximately 1 ms start up time before, an approximately 1 ms data storage time after and finally an approximately 20 ms read out time (see fig.: 1).

1.1 The KPiX yml file

The settings for the fpga and the kpix readout chip are given by a yml file. The options are given in the table below

Table 1: DesyTrackerRunControl

Option	Decsription	Value range
CalMeanCount	Number of baseline values to be taken during Calibration	No Limit
CalDacMax	Sets upper DAC limit of calibration point for charge injection	0-255
CalDacMin	Sets lower DAC limit of calibration point for charge injection	0-255
CalDacStep	Describes the step size of the DAC value injection (1 = Every DAC value)	1-255
CalDacCount	Number of repeat injections for each DAC value	No Limit
CalChanMax	Sets end channel to be calibrated	0-1023
CalChanMin	Sets start channel to be calibrated	0-1023
runRate	Sets the acquisition frequency. Can be set to "auto" to have maximum rate Below are internal software variables holding current state. Not actual variable for changing in yml	1-30Hz/auto
CalState	Variable holding status of calibration (such as inejction)	
CalChannel	Variable holding current calibration channel value	
CalDac	Variable holding current calibration DAC injection value	

Table 2: DesyTracker

Option	Decsription	Value range
DesyTracker enable	Whether the entire block is enabled or not	True/False
AxiVersion enable	Whether the entire block is enabled or not	True/False
ScratchPad	32-bit test register in FPGA firmware so that software to verify it can talk to FPGA	0x000000
TluMonitor enable	Whether the entire block is enabled or not	True/False
ClkSel	Which clock should be used to generate the 200 MHz baseline	EthClk/TluClk
KPixDaqCore enable	Whether the entire block is enabled or not	True/False
SysConfig enable	Whether the entire block is enabled or not	True/False
RawDataMode	Debug mode that makes the firmware produce output data even if a channel/bucket has no hits	True/False
AutoReadDisable	Can be set to True in order to force the sending of a command to KPiX before it begins the readout	True/False
KPixClockGen enable	Whether the entire block is enabled or not	True/False
ClkSelReadout	Sets the readout clock period in units of $10\,\text{ns} \cdot ([value] + 1)$	4-255
ClkSelDigitize	Sets the digitize clock period in units of $10\,\text{ns} \cdot ([value] + 1)$	4-255
ClkSelAcquire	Sets the acquisition clock period in units of $10\,\text{ns} \cdot ([value] + 1)$	4-255
ClkSelIdle	Sets the acquisition clock period in units of $10\,\text{ns} \cdot ([value] + 1)$	4-255
ClkSelPrecharge	Sets the acquisition clock period in units of $10\,\text{ns} \cdot ([value] + 1)$	4-4095
SampleDelay	Controls the sample point by adding a delay in number of clock cycles before DATA line is sampled. E.g. 3 means data line will be sampled $(3 + 1) \cdot 5\,ns$ (200 MHz clock) cycles after each rising edge of the KPiX clock	0-255
SampleEdge	Sets whether to sample on rising or falling Edge	Rise/Fall
AcquisitionControl enabel	Whether the entire block is enabled or not	True/False
ExtTrigSrc	Source for the external trigger Signal	Disabled/BncTrig/Lemo0/Lemo1/ TluSpill/TluStart/TluTrigger/ EthAcq/EthStart
ExtTimestampSrc	Source for the external timestamp Signal	Same as above
ExtAcquisitionSrc	Source for the external signal to start Acquisition	Same as above
ExtStartSrc	Source for an external run start signal	Same as above
Calibrate	Whether it is a Calibration run or not	True/False
KpixAsicArray enable	Whether the entire block is enabled or not	True/False
KpixAsic[*] enable	Whether a specific Kpix block is enabled	True/False
CfgAutoReadDisable	When set to true KPiX only begins Data readout when a command is sent to it.	True/False

Table 3: DesyTracker

Option	Decsription	Value range
CfgForceTemp	Force whether Kpix temperature data should be read out (?)	True/False
CfgDisableTemp	Disable Kpix temperature module	True/False
CfgAutoStatusReadEn	(?)	True/False
TimeResetOn	Set the number of cycles from the start of an acquisition cycle to wait before asserting reset.	0-[TimeBunchClkDelay
TimeResetOff	Set the number of cycles from the start of an acquisition cycle to wait before setting reset back to zero	[TimeResetOn]-[TBCD]
TimeOffsetNullOff	Offsets of the system are sampled by switching all discriminators into a follower mode and impressing the levels into capacitors at the inverting inputs of the discriminators. This is a kind of double correlated sampling applied to the full acquisition cycle. At OffsetNullOff the follower mode is terminated.	0-[TBCD]
TimeLeakageNullOff	Leakage compensation for DC coupled sensor	0-[TBCD]
TimeDeselDelay	Time at which the desel_all_cells signal is asserted to the analog side of KPiX	0-[TBCD]
TimeBunchClkDelay	Sets the duration of the start up phase in units of MCC (acq.clock periods)	0-Uint16
TimeDigitizeDelay	How many clock cycles to wait between acquisition and digitization. (Affects synchronization for unknown reasons)	0-(?)
TimePowerUpOn	Set on which MCC analog power net currents are raised to operative levels	0-[TBCD]
TimePowerUpDig	Set on which MCC digital power net currents are raised to operative levels	0-[TBCD]
TimeThreshOff	At this time a threshold is applied to the bottom terminal of the capacitor holding the offset level. In the current version of KPiX some buffers get very slow due to power drops on busses and the transition from follower to discriminator takes time.	0-[TBCD]
TrigInhibitOff	How many BunchClockCounts (BCC) of the acquisition a trigger should be suppressed	0-8191
BunchClockCount	How many BCC the acquisition phase should last for	0-8191
Cal0Delay	Delay in BCC on when first calibration DAC injection happens	0-8191
Cal1Delay	Delay in BCC on when second calibration DAC injection happens relative to the first	0-8191
Cal2Delay	Delay in BCC on when third calibration DAC injection happens relative to the second	0-8191
Cal3Delay	Delay in BCC on when fourth calibration DAC injection happens relative to the third	0-8191
CalCount	How many buckets should be Calibrated	1-4

Table 4: DesyTracker

Option	Decsription	Value range
DacRampThresh	Wilkinson converter threshold. Can be raised to generate a offset for conversion result	0-255
DacRangeThreshold	Signal amplitude at which the dynamic switch to enables the 10 pF capcitor	0-255
DacCalibration	Sets the calibration amplitude but is overwritten in calibration to run through prescribed cycle	0-255
DacEventThreshold	Internal bias level, not to be changed	-
DacShaperBias	Bias level of the shaper, not to be changed	-
DacDefaultAnalog	A bias level impressed on the analog bus before connection to the analog storage capacitor	(?)
DacThresholdA	Setting the DAC threshold level for threshold A which is used in self triggering	0-255
DacThresholdB	Setting the DAC threshold level for threshold B which is used in self triggering	0-255
CntrlDisPerReset	Option for a periodic reset in synchronism with the ILC bunch structure is disabled	True/False(?)
CntrlEnDcReset	Enables DC reset used for all non-synchronous data	True/False(?)
CntrlHighGain	Set whether the system should operate in high gain	True/False
CntrlNearNeighbor	Option to trigger a neighboring pixel even if it is below threshold. Only partially matched layout of tracker and requires changes.	True/False
CntrlCalSource	Set which calibration level should be used (external not in use)	Disable/ Internal/ External
CntrlForceTrigSource	Force trigger to be of a certain type	Disable/ Internal/ External
CntrlHoldTime	Sets how long the signal should be sampled in units of BCC (8x = 1 BCC, 40 = 2 BCC etc.)	Increasing order (8x, 40x, 24x, 56x, 16x, 48x, 32x, 64x)
CntrlCalibHigh	Whether to enable the the parallel 5 pF capacitor in the calibration injection for bucket 0	True/False
CntrlShortIntEn	Option to reduce integration time for data in the storage capacitors from 0.5 to 0.2 μs	(?)
CntrlForceLowGain	Set whether the system should operate in low gain Setting both CntrlForceLowGain and CntrlHighGain to False operates the system in normal gain	True/False
CntrlLeakNullDisable	Disabled leakage null compensation entirely	True/False
CntrlPolarity	Set polarity of input signals	Positive/Negative (normally set to Positive)
CntrlTrigDisable	Disable self triggering of KPix	True/False
CntrlDisPwrCycle	Disable power cycling of the champ (no shut off phase)	True/False
CntrlFeCurr	Sets the current in the frontEnd	0-(?)uA (unit is important)

Table 5: DesyTracker

Option	Decsription	Value range
CntrlDiffTime	Sets the differentiation time to the shaper (?)	Normal/Half/ Third/Quarter
CntrlMonSource	Option to bring out two analog signals from channel 8. Will be removed with next submission	None/Amp/Shaper
Chan_0_31	Used to manually disable channels (D) or set them to Thresholds (A/B) or to Calibrate (C), 32 channels per row, example: AAADAAAA ... means channel 3 is disabled	A/B/C/D
KpixAsic[X] enable	Sets whether the system should expect a KPIX in slot X	X=0-24 (but 24 always needs to be True for the virtual KPIX on the FPGA board) True/False
KpixDataRxArray enabel	Whether the entire block is enabled or not	True/False
KpixDataRx[*] enable	Whether data should be sent out by the KPiX in all slots (wildcard) (?)	True/False (should always be True)