ILC Vertex Detectors & Silicon Trackers

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On behalf of the ILD and SiD detectors R&D groups
Outline

- The International Linear Collider
- ILC Detector Challenges
- Current vertex detector & tracking systems design
- R&D efforts
- Summary and Outlook
The International Linear Collider (ILC)

- $\text{e}^+\text{e}^-$ Linear Collider 31 km long with baseline $\sqrt{s} = 500 \text{ GeV}$
  - Phases @ 250 & 350 GeV
  - Possible Upgrade @ 1TeV

- Baseline beam parameters
  - $2 \times 10^{10}$ parts/bunch spaced by 554 ns
  - Polarization 80/30 for e-/e+
  - $L = 1.8 \times 10^{34} \text{ cm}^2\text{s}^{-1}$

- 2 Detectors in “push and pull”: ILD & SiD

Brief history, Current Status & prospects

- **2012**: TDR and Detailed Baseline Design (DBD)
- **Fall 2015**: High-ranking US-Japan Talk starts
- **May 2016**: KEK Management “Japanese Decision on ILC will be Input to the European Strategy”
- **Dec. 2016**: E-XFEL goes online
- **2017**: Staging discussion ⇒ start @ 250 GeV to reduce cost?
- **Green Light ⇒ International Laboratorys**
ILC Key Features & Physics Goals

Key features
- Well known initial state, no QCD background, fully reconstructible channels
- Precise theoretical predictions: radiation corrections O(1%) & theoretical error O(0.1%)
- Tunable $\sqrt{s}$ (threshold scan & flexibility) & Beam polarization (S/N enhancement)
- Globally small cross-section but highly pure samples
- Advantages: triggerless, low backgrounds, most measurement statistically limited

Very rich physics program
- Higgs sector
  - O(1%) precision of mass/width/spin & couplings
  - Model independent measurements ($\sigma$ & $\sigma \times \text{Br}$)
      $\Rightarrow$ Probe BSM, model disentangling
- Top physics
- EW precision measurements
- Direct/indirect BSM searches

Very important role of Vertex detector
- Favour tagging ($b$, $c$, $\tau$)
- Low momentum tracking (as lows as 200 MeV/c)
- Jet charge determination
ILC Experimental Environment

Beam structure
- 5 trains/s of ~1300/2600 bunches
- 1 bunch every 550/370 ns
- Beam-less time ~ 200 ms
- Operation strategies
  - Full detector readout (r.o.) ⇒ triggerless
  - Possible r.o. during beam-less time
  - Power pulsing ⇒ reduced power

Beam induced bkg: Beamstrahlung
- Beam energy loss: ~1% @ 250 GeV
- Radiation level: ~100kRad \( \oplus 10^{11} \) \( n_{eq} \)/cm\(^2\)
  (HL-LHC: ~1GRad \( \oplus 10^{16} \) \( n_{eq} \)/cm\(^2\))
- Low momentum (10 – 100 MeV/c) real tracks!
- Main occupancy source: drives VTX r.o. speed & \( R_{min} \)
- Typical rate of ~ 6 hits/cm\(^2\)/BX on innermost VTX layer
- Large systematic uncertainty
  ⇒ Safety factor of at least x5 needed
ILC Detector Challenges

- Detector design driven by running conditions and physics goals
  - **Strategy:** use of particle flow algorithms used to an unprecedented level

- For this need an unprecedented precision detectors
  - Jet $\sigma_E$
    - factor of 3 improvement on jet $\sigma_E$ w.r.t. LHC (~200 higher calorimeter granularity)
  - **Tracking and Vertexing**
    - Momentum resolution factor of 10 w.r.t. LHC
    - Track pointing to IP
    - Low momentum tracking ($p_T \lesssim 100$ MeV/c)
    - Enhanced flavour $(b, c, \tau)$ tagging: short lived particles flying $O(100 \, \mu m)$
    - All this achieved with 10-20 finer pixels and ~5-10 lower Mat. Budget w.r.t. LHC

- Other performances much less demanding w.r.t. LHC
  - Radiation hardness
  - Time resolution
  - Data rate
ILC Detector Design: 2 complementary approaches

Common approach
- Allow push pull
- Exploit fully Particle Flow Algorithms

Common features
- SiW EMcal & Hcal inside coil
- Muon detector
- Forward trackers
- Low mass vertex detectors

long barrel

shorter barrel with endcap disks

Larger
- optimizes PFA (particle separation)
- 3.5 Tesla
- TPC
- dE/dx
- Large number of hits \Rightarrow pattern recognition

Size
- Magnetic field
- Main tracker

More compact
- 5 Tesla
- Silicon only
- optimizes vertex performances
- compensates smaller size
- more costs efficient
- robustness, time stamping
- few high precision points

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ILC Vertex Detector (VTX) Requirements

- **Linear e⁺e⁻ collider**
  - Exhibit milder running conditions than pp/LHC
    - Relaxed readout-speed & radiation tolerance
  - Favours technologies focusing on resolution & material budget

- **VTX requirements**
  - Physics performances: \( \sigma(d_0) < 5 \oplus 10/p\beta \sin^{3/2}\theta \ \mu m \)
    \( \Rightarrow \sigma_{sp} \approx 3 \ \mu m \) (~17 \ \mu m pitch) & low material budget (~0.15% \( X_0 \)/layer)
  - Occupancy \( \Leftrightarrow \) readout-speed: few % occupancy (~6 hits/cm\(^2\)/BX)
  - Moderate radiation tolerance (/year): \( \sim 100\text{kRad} \oplus 10^{11} \text{n}_{eq}/\text{cm}^2 \)
  - Power dissipation \( \Leftrightarrow \) preferably air cooling: 600W/12W (power cycling, 3% duty cycle)
  - Readout & electronics
    - Immunity to SEU and Latchup
    - Highly integrated readout \( \mu \)-circuits & high data transfer rate (triggerless)
  - Other parameters
    - Cost, fabrication reliability and flexibility
    - Mechanical integration: low mass, rigidity and heat conductive
    - Alignment: sub-micron level

- **Reach the specifications all together is the real challenge**
SiD: VTX and Silicon Strip tracker

**Silicon Strip Tracker**
- All silicon tracker
- Use silicon micro-strips and double metal layers
- 5 barrel + 4 disks
- Gas cooled
- Material budget less than 20% $X_0$ in active area
- Readout KPIX ASIC bump-bonded to modules

**VTX**
- 5 barrel pixel + 7 disks (4 close and 3 far away)
- Baseline: pixel pitch $20 \times 20 \, \mu m^2$
- **Technology options**
  - Monolithic CMOS chip ⇒ **Chronopix**
  - 3D vertically integrated silicon
ILD: VTX and Silicon Tracking System

- **Silicon Inner & External Trackers (SIT & SET)**
  - Si-strip detectors: 200 µm thick, 50 µm pitch, 10×10 cm² sensors, edgeless, 7 µm $\sigma_{sp}$
  - Improves resolution and linking VTX-Tracker-Ecal

- **Fwd Tracker (FTD):** 7 disks (2 pixel & 5 Si-strips)
  - 2 closest layers: small pixels 20×20 µm² ($\sigma_{sp}$ ~4 µm) $\Rightarrow$ DEPFET
  - 5 farthermost layers: strips similar to SIT/SET

- **Barrel (VTX):** 3 × double-sided-ladders
  - Inner layers (< 300 cm²): priority r.o. speed & $\sigma_{sp}$
    - 16×16/80 µm² pixels & binary output: $t_{r.o.}$ ~50/8 µs & $\sigma_{sp}$ ~3/5 µm
  - Outer layers (~3000 cm²): priority to power consumption & $\sigma_{sp}$
    - 35×35 µm² pixels & 3-4 bit charge encoding: $t_{r.o.}$ ~100 µs & $\sigma_{sp}$ ~4 µm
  - R&D on several technologies $\Rightarrow$ DEPFET, FPCCD, SOI, CMOS

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Targeted Tracking System Material Budget

$X_0$ vs polar angle

- **Goal**: $\sim 10\% X_0$ for complete tracker in barrel region $\Rightarrow$ very challenging

- **Comparison with ATLAS barrel region**
  - Current tracker: $\sim 50\% X_0$
  - ATLAS ITK: $\sim 30\% X_0$
ILC Tracking system expected performances: I.P. resolution

- Results from full simulation single muon particle gun
  - $\sigma_{sp}$ 1st VTX layer $\sim 3$ $\mu$m
  - Mat. Buget/layer $\sim 0.15% X_0$
  - Beam pipe: Be 500 $\mu$m (0.14% $X_0$)
  - Empirical parametrization

  **ILC:** $\sigma(d_0) = a \oplus b/p\beta \sin^{3/2}\theta \mu$m

<table>
<thead>
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<th>LEP</th>
<th>SLC</th>
<th>LHC</th>
<th>RHIC</th>
<th>ILC</th>
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<tr>
<td>$a$ ($\mu$m)</td>
<td>25</td>
<td>8</td>
<td>12</td>
<td>13</td>
<td>5</td>
</tr>
<tr>
<td>$b$ ($\mu$m GeV/c)</td>
<td>70</td>
<td>33</td>
<td>70</td>
<td>19</td>
<td>10</td>
</tr>
</tbody>
</table>
Solving the fill factor of strips LGAD
- No segmentation of multiplication layer
- Segmentation of ohmic contact → collect holes
- Detector could be very thin (35 – 40 μm)
  - Small material budget
  - Good timing (few 10s ps for hole collection)
- Interesting application for ILD SIT tracker layers

First ever multi-channel tracking module based on Strip I-LGAD & LGAD
- 160 μm pitch & ~300 μm thickness

IFCA (Santander) CNM

IFCA (Santander) CNM

I-LGAD concept

Gain ≡ MPV I-LGAD / MPV reference PIN

@ -22 C
(Biased by The gain temperature Dependence of the beetle ROC)

@ Room temp.
Reducing Material Budget: Technical developments

Power consumption & Cooling
- Baseline: air cooling (few 10s of W)
  - Goal: ≤ 20 mW/cm²
- Requirements: technology dependent
  - Baseline: air flow (few m/s) + power pulsing
  - DEPFET: FEE μ-channel cooling
  - FPCCD: requires -40°C ⇒ (2 phase-CO₂)
  - CMOS: asynch. r.o.: maybe no power pulsing

Sensor integration in ultra-light devices
- Beam-pipe: Be 500 μm (0.14% X₀)
- 50 μm thick sensors routinely produced
e.g. CMOS, DEPFET, …
- Today: 0.2 – 0.4 % X₀/layer in acceptance
- 0.15% X₀/layer seems reachable!

See P. Petagna (Overview), A. Mapelli (NA62), O. Aguilar (LHCb) Talks
ILD & SiD share Vertex Detector R&D
- Several mature technos. considered needing more R&D to meet requirements
- Safety margin uncertainty mainly from beam bkg knowledge
  - Large systematics and depends on beam-energy and IR design

No technology yet chosen
- Still have some time and all technologies still evolving
- Selection based on physics benchmarks performances
- Different geometries are being considered
  - 3 x double-sided-ladders vs 5 single-sided?
  - Long or short barrel + disks?
- Different r.o. strategies
- Performances obtained with technology/geometry specific tracking/vertexing algorithms

Several options still on the table
### VTX Readout Strategies

<table>
<thead>
<tr>
<th>Power</th>
<th>Time resolution</th>
<th>Spatial resolution</th>
<th>Advantages</th>
<th>Caveats</th>
</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>1 complete train</td>
<td>~1 μm</td>
<td>Spatial Resolution&lt;br&gt;Hit separation&lt;br&gt;Beam background tagging capabilities ? (cluster shapes)</td>
<td>(\Rightarrow) x16 #pixels to read-out in 200ms&lt;br&gt;(\Rightarrow) No time stamping&lt;br&gt;(\Rightarrow) Occupancy issues ?</td>
</tr>
</tbody>
</table>

In pixel circuitry to store hits with **time stamping** (e.g. chronopixels, SOI)

<table>
<thead>
<tr>
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</tr>
</thead>
<tbody>
<tr>
<td>Low</td>
<td>Single or few bunches (&gt;~ 0.5 μs)</td>
<td>~5 μm</td>
<td>Hit time stamping&lt;br&gt;Well suited to outer layers</td>
<td>(\Rightarrow) BX time stamping storage in conflict with granularity</td>
</tr>
</tbody>
</table>

**Continuous read-out during train** (e.g. DEPFET, CMOS): rolling shutter or priority encoding.

<table>
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</table>
| High  | Few to 10s bunches (5-50 μs) | ~3 μm              | Time & spatial resolution compromise | Power cycling mandatory ?
\(\Rightarrow\) F(Lorentz) ~ 10^8 grams
\(\Rightarrow\) Distribute 100s Amps shortly before train
\(\Rightarrow\) heat cycles the ladders. |

- Figures may evolve significantly with R&D and access to new technologies
  - e.g. feature size
  - Power, read-out speed, granularity, etc.
- Different options / room for mixed strategies ?
  - e.g. double sided ladders: 1-fast / 1-precise
**Design features**
- Monolithic CMOS pixel detector
- In-pixel
  - Pre-amp + Discri with offset compensator
  - Time-stamping (bunch-tagging) up to 2 hits (14-bits)
- Sparsified r.o. between trains

**R&D efforts**
- 3 sets of small prototypes since 2008
- Chronopix 3: 25x25 μm² in TSMC 90 nm CMOS (2015)
- Set of prototypes showed
  - Time-steping better than 300 ns proven
  - Sparsified readout architecture works
  - Power pulsing tested
  - Noise & cross-talk controlled
- Next steps
  - No show stoppers for full-size prototype
  - Still several optimizations of design
Studies with small prototypes with 6x6 μm² pixel
- Small prototypes 6x6 mm² thinned to 50 μm
- 4 channels with diff. register size: 6, 12, 18, 24 μm
- Prototype sufficiently radiation hard

Large prototype
- Real size sensor 12.3 x 62.4 mm² for double-sided ladder
- 125 x 13000 pixels with 16 r.o. nodes
- Readout ASIC prototype (TSMC 250 nm CMOS)
  - Between train r.o.
  - Amp+LPF+CDS+ADC+LVDS driver
  - 10 MHz r.o., 6 e⁻ noise, 5.6 mW/channel
- FPCCD + r.o. chip: 44 e⁻ noise
- Mechanics: Carbon fibre and flex
- Operates @ -40°C: CO₂ cooling

Next steps
- Beam-tests, ladders assembly + cooling
- Improve readout speed
**DEPFET**

**Development driven by Belle-II PXD**
- Ladder assembly qualified
- PXD modules currently in 1st pre-production batch
- SuperKEKB commissioning phase 2 (low lumi)
  - One sector of PXD will be installed
  - Machine bkg measurements & system validation

**Thin DEPFET for ILC**
- ILC prototypes manufactured
- 0.15% $X_0$ seems achievable: including switcher chips
- Resolution studies in simulation and Beam-test
- $\mu$-channel cooling under development
- Interest in pixelated FTD, and maybe VTX
- Next Steps: r.o. speed and integration

See J. Dingfelder Talk
SOFIST: SOI sensor for Fine measurement of Space and Time

Goal: fine pixels (~20x20 μm²) & bunch time-stamping

SOFIST v1: delivered Dec. 2015
- Chip size 2.9x2.9 mm² (pixel 20x20 μm²)
- Pre-amp (CSA) + Analog memories (2 hits)
- Column ADC (8 bits)
- FZ n-type (single SOI)
- TB @ Fermilab: σ_{sp} ~ 1.5 μm

SOFIST v2: delivered Jan. 2017
- Chip size 4.5x4.5 mm² (pixel 25x25 μm²)
- Pre-amp + Comp + Shift register + Analog memories (2 hits)
- Column ADC (8 bits) + Zero-suppression
- Cz p-type (double SOI)
- Under evaluation

SOFIST v3 & 4: under design, submission June 2017
- Chip size 6x6 & 4.5x4.5 mm² (pixel 30x30 & 20x20 μm²)
- Pre-amp + Comp + Shift register + Analog memories (3 hits)
- Column ADC (8 bits) + Zero-suppression
- FZ p-type (double SOI)

See K. Hara Talk for SOI recent developments

Osaka University, Tsukuba University, Tohoku University, KEK

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- Fine pixels (~20x20 μm²) & bunch time-stamping

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CMOS Pixel Sensors (CPS)

CPS for ILC
- Exploit potential of available CMOS technologies
- R&D performed in synergy with several applications
  - EUDET-BT, STAR, ALICE & CBM
- CPS is unique technology being simultaneously
  - Granular, thin, integrating full FEE, industrial & cheap
- Address trade-off between spatial resolution & r.o. speed

Current developments
- Driven by ALICE-ITS and CBM-MVD
  - Tower-Jazz 180 nm CMOS process
  - In pixel pre-amp + discrim. & asynchronous r.o.
- Focus on increased r.o. speed: few $\mu$s $\Rightarrow$ bunch tagging
  - To comply with beam bkg uncertainties
- Keep low power consumption
  - Potential to avoid power pulsing
- Radiation tolerance $>>$ needed for ILC
- Potential use for trackers (large surfaces)
  - Large pixels detection efficiency demonstrated

See G. Contin Talk

See A. Alici Talk
Summary and Outlook

ILC is a Mature Project
- Accelerator TDR
- ILD & SiD: feasibility of detectors demonstrated in DBD document in 2012

Vertex and Tracking Detectors
- Many options still available: technologies, r.o. architecture, geometries, ...
- Several experiments already approaching ILC specifications: ALICE, CBM, Belle-II, ...
- R&D still very active
  - Detector performances
  - Robustness w.r.t beam background & √s program
  - Careful mechanical integration studies
  - Tracking & Vertexing performances

What's next?
- Scientific environment & political opportunities for Japan ⇔ rest-of-the-world
- Coming years
  - Refine requirements & prioritize physics goals
  - On the road for ILD & SiD TDR
Backup
Physics @ ILC: Key Features

- **Clean Environment**
  - No QCD background $\Rightarrow$ no pile up
  - Well known initial state
  - Fully reconstructible channels (even fully hadronic)

- **Precise Theoretical Predictions**
  - Radiative corrections $O(1\%)$
  - Theoretical uncertainties $O(0.1\%)$

- **Tunable $\sqrt{s}$ ⇔ Threshold scans & flexibility**

- **Beam polarization ⇔ S/N enhancement**

- **Cross sections**
  - Globally small ($\sigma_{ZH} \sim 100$ fb) but ...
  - Higgs production @ LHC: $1/10^{10}$ events
  - Higgs production @ ILC: $1/10^2$ events

- **Advantages**
  - Triggerless
  - Low backgrounds
  - Most measurements statistically limited
Physics @ ILC: Goals

- **Very rich physics program**
  - Top physics
  - EW precision measurements
  - Direct/indirect BSM searches

- **Higgs sector**
  - $O(1\%)$ precision of Higgs mass/width/spin & couplings
  - Model independent measurements
    - Access $\sigma$ and $\sigma \times \text{Br}$
    - Probe BSM, model disentangling

- **Very important role of Vertex detector**
  - Favour tagging ($b$, $c$, $\tau$)
  - Low momentum tracking (as low as 200 MeV/c)
  - Jet charge determination
Physics @ ILC: BSM example

- Is the O(1%) precision on Higgs couplings enough
- Size of deviation depends on BSM mass scale
- Correlations of Higgs couplings deviation from SM allows to disentangle new physics models

\[
\frac{g_{bb}}{g_{SM bb}} = \frac{g_{b\tau\tau}}{g_{SM b\tau\tau}} \simeq 1 + 1.7\% \left( \frac{1 \text{ TeV}}{m_A} \right)^2 \quad \text{heavy Higgs mass}
\]
ILC Experimental Environment

**Beam structure**
- 5 trains/s of ~1300/2600 bunches
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- Beam-less time ~ 200 ms
- Operation strategies
  - Full detector readout (r.o.) \(\Rightarrow\) triggerless
  - Possible r.o. during beam-less time
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**Beam induced bkg: Beamstrahlung**
- Beam energy loss: ~1% @ 250 GeV
- Radiation level: \(\sim 100\text{kRad} \oplus 10^{11} \text{n}_{eq}/\text{cm}^2\)
  - (HL-LHC: \(\sim 1\text{GRad} \oplus 10^{16} \text{n}_{eq}/\text{cm}^2\))
- Main source of occupancy
  - Drives VTX r.o. speed & minimum radius
  - Physics cross section negligible (~ 1 evt/s)
ILC Experimental Environment: Beam Bkg on ILD

Beam Bkg Simulation (Guinea Pig)
- $e^+e^-$ pairs production
- $\sqrt{s}$ dependent rates
- ~20% rates due to back scatterers
- Stat-only error, systematics much higher

Some features
- Low momentum (10 – 100 MeV/c) real tracks!
- Typical rate of ~ 6 hits/cm²/BX on innermost VTX layer
- Very sensitive to IR design
- Large systematic uncertainty
  ⇒ Safety factor of at least x5 needed

<table>
<thead>
<tr>
<th>Sub-detector</th>
<th>Units</th>
<th>Layer</th>
<th>TDR ws 500 GeV</th>
<th>B1b ws 1000 GeV</th>
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<tbody>
<tr>
<td>VTX-DL</td>
<td>hits/cm²/BX</td>
<td>1</td>
<td>6.320 ± 1.763</td>
<td>11.774 ± 0.992</td>
</tr>
<tr>
<td></td>
<td></td>
<td>2</td>
<td>4.069 ± 1.176</td>
<td>7.479 ± 0.747</td>
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<tr>
<td></td>
<td></td>
<td>3</td>
<td>0.250 ± 0.109</td>
<td>0.431 ± 0.128</td>
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<tr>
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<td>4</td>
<td>0.212 ± 0.094</td>
<td>0.360 ± 0.108</td>
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<td>5</td>
<td>0.048 ± 0.031</td>
<td>0.091 ± 0.044</td>
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<tr>
<td></td>
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<td>6</td>
<td>0.041 ± 0.026</td>
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<td>0.046 ± 0.017</td>
<td>0.102 ± 0.016</td>
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<td>3</td>
<td>0.025 ± 0.009</td>
<td>0.070 ± 0.009</td>
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<td>0.016 ± 0.005</td>
<td>0.046 ± 0.007</td>
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<td>0.011 ± 0.004</td>
<td>0.034 ± 0.005</td>
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<td>6</td>
<td>0.007 ± 0.004</td>
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<td>7</td>
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<td>0.196 ± 0.924</td>
<td>0.588 ± 2.406</td>
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<td>2</td>
<td>0.239 ± 1.086</td>
<td>0.670 ± 2.616</td>
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<td>TPC</td>
<td>hits/BX</td>
<td>-</td>
<td>216 ± 302</td>
<td>465 ± 356</td>
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<tr>
<td>ECAL</td>
<td>hits/BX</td>
<td>-</td>
<td>444 ± 118</td>
<td>1487 ± 166</td>
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<tr>
<td>HCAL</td>
<td>hits/BX</td>
<td>-</td>
<td>18049 ± 729</td>
<td>54507 ± 923</td>
</tr>
</tbody>
</table>
The ILC Machine

- **500 GeV Linear collider**
  - 31 km long
- **Acceleration**
  - 7400 superconducting Cavities in 850 Cryo Modules
  - Gradient 31.5 MV/m
  - 1.3 GHz RF
  - 163 MW power consumption
- **Beam parameters**
  - $2\times10^{10}$ particles/bunch
  - 554 ns spacing
  - $L=1.8\times10^{34} \text{ cm}^{-2}\text{s}^{-1}$
  - Polarization 80/30 ($\text{e}^-/\text{e}^+$)
  - Nanometer-scale beam spot
ILC Site – Kitakami Mountains

IP: (underground) candidate Location:
Proposed by JHEP community
Endorsed by LCC
Not decided by Japanese Government

High-way
Express-Rail

Sendai
Ichinoseki
Oshu

Ofunato
Kesen-numa

Hitokabe Granite
Senmaya Granite
Orikabe Granite

BDS, DR, DH
ILC baseline program

Integrated Luminosities [fb]

ILC, Scenario H-20
- ECM = 250 GeV
- ECM = 350 GeV
- ECM = 500 GeV

Luminosity Upgrade

Integrated luminosities

years

0 5 10 15 20

0 1000 2000 3000 4000
SiD: vertex detector

- **Layout:**
  - Short barrel approach
  - Barrel: 5 silicon pixels layers
  - Forward disks
    - 4 disks at short distance
    - 3 disks at longer distance

- **Technology options**
  - Baseline
    - pixels pitch: 20 x 20 μm²
  - CMOS based Chronopixels
    - In pixel 12 bits time stamping
    - Read-out between trains
    - Reduce beam background
    - Allows tracking with VTX seeding
    - Requires very advanced technology (90 nm)
  - 3D vertical integrated silicon
    - Even more challenging

<table>
<thead>
<tr>
<th>Barrel</th>
<th>R</th>
<th>z_{max}</th>
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<tbody>
<tr>
<td>Layer 1</td>
<td>14</td>
<td>63</td>
</tr>
<tr>
<td>Layer 2</td>
<td>22</td>
<td>63</td>
</tr>
<tr>
<td>Layer 3</td>
<td>35</td>
<td>63</td>
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<tr>
<td>Layer 4</td>
<td>48</td>
<td>63</td>
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<tr>
<td>Layer 5</td>
<td>60</td>
<td>63</td>
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</table>

<table>
<thead>
<tr>
<th>Disk</th>
<th>R_{inner}</th>
<th>R_{outer}</th>
<th>z_{center}</th>
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</thead>
<tbody>
<tr>
<td>Disk 1</td>
<td>14</td>
<td>71</td>
<td>72</td>
</tr>
<tr>
<td>Disk 2</td>
<td>16</td>
<td>71</td>
<td>92</td>
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<tr>
<td>Disk 3</td>
<td>18</td>
<td>71</td>
<td>123</td>
</tr>
<tr>
<td>Disk 4</td>
<td>20</td>
<td>71</td>
<td>172</td>
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</table>

<table>
<thead>
<tr>
<th>Forward Disk</th>
<th>R_{inner}</th>
<th>R_{outer}</th>
<th>z_{center}</th>
</tr>
</thead>
<tbody>
<tr>
<td>Disk 1</td>
<td>28</td>
<td>166</td>
<td>207</td>
</tr>
<tr>
<td>Disk 2</td>
<td>76</td>
<td>166</td>
<td>541</td>
</tr>
<tr>
<td>Disk 3</td>
<td>117</td>
<td>166</td>
<td>832</td>
</tr>
</tbody>
</table>
ILD tracking system: TPC + silicon (1)

- **Main system: TPC**
  - 2 options: GEMs/Micromegas
- **Silicon Strip detectors**
  - 200\(\mu\)m thick silicon, 50 \(\mu\)m pitch, 10x10cm\(^2\) sensors, edgeless, 7\(\mu\)m sp.res.
  - 4 components
    - Silicon inner Tracker (SIT)
    - Silicon External Tracker (SET)
    - End cap Tracker (ETD)
    - Forward Tracker (FTD)
  - Goals:
    - Improves resolution
    - Linking VTX-Tracker-ECal
    - Improves calibration, alignment
    - Allows time stamping
  - Challenges and R&D:
    - maintain the mat.budget small
    - push pull compatible
    - minimize power (power pulsing)

<table>
<thead>
<tr>
<th>Performance/Design Goals</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Momentum resolution* at (B=3.5)T</td>
<td>(\delta(p_t) \approx 10^{-4}/\text{GeV/c} ) TPC only</td>
</tr>
<tr>
<td>Solid angle coverage</td>
<td>Up to (\cos \theta \approx 0.98) (10 pad rows)</td>
</tr>
<tr>
<td>TPC material budget</td>
<td>(\approx 0.05X_0) including the outer field cage in (r) and (&lt; 0.25X_0) for readout endcaps in (z)</td>
</tr>
<tr>
<td>Number of pads/timebuckets</td>
<td>(\approx 1 \times 10^9/1000) per endcap</td>
</tr>
<tr>
<td>Pad pitch/no.paddrows</td>
<td>(1 \times 4-10\ mm \approx 200)</td>
</tr>
<tr>
<td>(\sigma_{\text{point}}) in (r_\phi)</td>
<td>(&lt; 100\mu)m (avg for straight-radial tracks)</td>
</tr>
<tr>
<td>(\sigma_{\text{point}}) in (r_z)</td>
<td>(&lt; 0.4-1.4\ mm) (for zero – full drift)</td>
</tr>
<tr>
<td>2-hit resolution in (r_\phi)</td>
<td>(&lt; 2\ mm) (for straight-radial tracks)</td>
</tr>
<tr>
<td>2-hit resolution in (r_z)</td>
<td>(&lt; 6\ mm) (for straight-radial tracks)</td>
</tr>
<tr>
<td>dE/dx resolution</td>
<td>(&lt; 5\ \text{%})</td>
</tr>
<tr>
<td>Performance</td>
<td>&gt; 97% efficiency (for TPC only (p_t &gt; 1\text{GeV/c}))</td>
</tr>
<tr>
<td>Background robustness</td>
<td>Full efficiency with 1% occupancy, Chamber prepared for 10-20% occupancy (at the linear collider start-up, for example)</td>
</tr>
</tbody>
</table>

\*The momentum resolution for the combined central tracker is \(\delta(p_t) \approx 2 \times 10^{-3}/\text{GeV/c}\)
ILD tracking system: TPC + silicon (2)

Radiation length vs polar angle

Number of hits vs polar angle

Goal: \( \sim 10\% X_0 \) for the complete tracker

| SIT characteristics (current baseline = false double-sided Si microstrips) |
|--------------------------|-----------------|-----------------|-----------------|
| Geometry | Characteristics | Material |
| R[mm] | Z[mm] | cos\( \theta \) | Resolution R-\( \phi \)[\( \mu \)m] | Time [ns] | RL[\%] |
| 153 | 368 | 0.910 | 307.7 (153.8) | 0.65 |
| 300 | 641 | 0.902 | | |

| SET characteristics (current baseline = false double-sided Si microstrips) |
|--------------------------|-----------------|-----------------|
| Geometry | Characteristics |
| R[mm] | Z[mm] | cos\( \theta \) | Resolution R-\( \phi \)[\( \mu \)m] | Time [ns] |
| 1811 | 2350 | 0.789 | 307.7 (153.8) | 0.65 |

| ETD characteristics (current baseline = single-sided Si microstrips, same as SET ones) |
|-----------------|-----------------|-----------------|
| Geometry | Characteristics |
| R[mm] | Z[mm] | cos\( \theta \) | Resolution R-\( \phi \)[\( \mu \)m] | RL[\%] |
| 419.3-1822.7 | 2120 | 0.985-0.799 | x:\( \sigma \)=7.0 | 0.65 |

| FTD characteristics (design baseline: pixels for two inner disks, microstrips) |
|--------------------------|-----------------|-----------------|-----------------|
| Geometry | Characteristics | Material |
| R[mm] | Z[mm] | cos\( \theta \) | Resolution R-\( \phi \)[\( \mu \)m] | RL[\%] | sigma |
| 39-164 | 220 | 0.985-0.802 | 0.25-0.5 |
| 49.6-164 | 371.3 | 0.991-0.914 | 0.25-0.5 |
| 70.1-308 | 644.9 | 0.994-0.902 | 0.65 |
| 100.3-309 | 1046.1 | 0.994-0.959 | 0.65 |
| 130.4-309 | 1447.3 | 0.995-0.998 | 0.65 |
| 160.5-309 | 1848.5 | 0.996-0.986 | 0.65 |
| 190.5-309 | 2250 | 0.996-0.900 | 0.65 |
ILD: Vertex detector

- **Layout (DBD geometry):**
  - Long Barrel approach
  - Radius: ~15 mm – 60 mm
  - 3 x double sided ladders
    - Optimize material budget / alignment.
    - Stand alone tracking improvement
    - Background tagging capabilities
    - Other option: 5 single sided layers
  - Layers 1 & 2:
    - Priority to read-out speed & spatial resolution
    - Small pixels: 17 x 17 / 33 \( \mu \text{m}^2 \)
    - Binary charge encoding
    - Read-out time \( \sim 50 / 8 \) \( \mu \text{s} \)
    - \( \sigma_{sp} \sim 3 / 5 \) \( \mu \text{m} \)
  - Layers 3 – 6
    - Optimized for power consumption
    - Large pixels (25/35 x 35 \( \mu \text{m}^2 \))
    - 3-4 bits charge encoding
    - Read-out time \( \sim 60 \) \( \mu \text{s} \)
    - \( \sigma_{sp} \sim 4 \) \( \mu \text{m} \)
CMOS Pixel Sensors (CPS): Main features

Assets of CPS

- Signal processing integrated on sensor substrate
  ⇒ downstream electronics & syst. Integration
- Standard fabrication process
  ⇒ low cost & easy prototyping, many vendors, …
- High granularity ⇒ excellent spatial resolution (O(μm))
- Signal generated in thin (10-40μm) epi-layer
  ⇒ usual thinning up to 50 μm total thickness

Application domain widens continuously (existing/foreseen/potential)

- Heavy-ion collisions
  - STAR-PXL, ALICE-ITS, CBM-MVD, NA61…
- e⁺e⁻ collisions
  - BES-III, ILC, Belle II (BEAST II)
- Non-collider experiments
  - FIRST, NA63, Mu2e, PANDA, …
- High-precision beam-telescopes (adapted to medium/low energy e⁺ beams)
  - Few μm resolution @ DUT achievable with EUDET-BT (DESY), BTF-BT (Frascati)
CPS State-of-the-Art in operation: STAR-PXL detector

**STAR-PXL @ RHIC**

1st CPS @ a collider experiment!

**ULTIMATE Sensor (Mimosa28)**
- Rolling shutter r.o. \( (t_{\text{r.o.}} \leq 200 \, \mu s) \)
- \( T_{\text{op}} = 30 – 35^\circ \text{C} \)
- \( \varepsilon_{\text{det}} \geq 99.9\% \) \( \sigma_{\text{sp}} \geq 3.5 \, \mu \text{m} \) & \( f_{\text{rate}} \leq 10^{-5} \)
- Rad. hard up to \( 150\text{kRad} \oplus 3 \times 10^{12} n_{\text{eq}} / \text{cm}^2 \)

**STAR-PXL HALF-BARREL (180M pixels)**
- 2 layers @ \( r = 2.8, 8 \, \text{cm} \)
- 20 ladders (10 sensors) \( (0.37\% \, X_0) \)

Several Physics-runs
- 1st / 2nd run in 2014 & 2015
- Preparation for 3rd run (Jan. 2016)
- \( \sigma_{\text{ip}} (p_T) \) matching requirements
  \( \sim 40 \, \mu \text{m} @ 600 \, \text{MeV}/c \) for \( \pi^\pm/K^\pm \)

Observation of \( D^0 \) production
- **STAR**: peak significance = 18
- **ALICE**: peak significance = 5
CPS performances: r.o. speed & rad. hardness

- 15 years of experience of PICSEL group in developing CPS
- Strong collaboration with ADMOS group at Frankfurt

- r.o. speed evolution
  - Two orders of magnitude improvement in 15 years of research

- Radiation tolerance
  - Significant improvement with time
  - Validation up to $10\,\text{MRad} \oplus 10^{14}\text{n}_{eq}/\text{cm}^2$
  - Adequacy to ALICE-ITS and CBM applications
CPS performances: Spatial Resolution ($\sigma_{sp}$)

Several parameters govern $\sigma_{sp}$

- **Pixel pitch**
- **Epi-layer**: thickness & $\rho$
- **Sensing node**: geometry & electrical properties
- **Signal-encoding resolution**: Nb of bits
- $\sigma_{sp}$ function of:
  - pitch $\oplus$ SNR $\oplus$ charge-sharing $\oplus$ ADC

**Pixel-pitch impact (analogue output)**
- Pitch = 10 (40) $\mu$m $\Rightarrow$ $\sigma_{sp}$ ~ 1 $\mu$m ($\leq$ 3 $\mu$m)
- Nearly linear improvement in $\sigma_{sp}$ vs pixel pitch

**Signal-encoding impact (digital output)**
- $\sigma_{sp}^{digi} = \text{pitch}/(12)^{1/2}$
- $\Rightarrow$ e.g. $\sigma_{sp}^{digi}$ ~ 5.7 $\mu$m for 20 $\mu$m pitch
- Significant improvement in $\sigma_{sp}$ by increasing signal encoding resolution

<table>
<thead>
<tr>
<th>Nb of bits</th>
<th>12</th>
<th>3-4</th>
<th>1</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Data</strong></td>
<td>measured</td>
<td>reprocessed</td>
<td>measured</td>
</tr>
<tr>
<td>$\sigma_{sp}$</td>
<td>$\leq$ 1.5 $\mu$m</td>
<td>$\leq$ 2 $\mu$m</td>
<td>$\leq$ 3.5 $\mu$m</td>
</tr>
</tbody>
</table>
**ALICE-ITS: Readout chain components**

### Typical readout components
- **AMP**: in-pixel low noise pre-amplifier
- **Filter**: in-pixel filter
- **ADC (1-bit $\equiv$ discriminator)**: may be implemented at end-of-column or pixel level
- **Zero suppression** (SUZE): only hit pixel info is retained and transferred
  - Implemented at sensor periphery (usual) or inside pixel array
- **Data transmission**: $O(\text{Gbps})$ link implemented at sensor periphery

### r.o. alternatives
- Rolling shutter (synchronous): $||$ column r.o. reading $N$-lines at the time (usually $N = 1-2$)
- data-driven (asynchronous): only hit pixels are output upon request (priority encoding)

### Rolling shutter: best approach for twin-well process
- Trade-off between performance, design complexity, pixel dimensions, power, ...
- e.g.: Mimosa-26 (EUDET-BT), Mimosa-28 (STAR-PXL)
Next challenge: ALICE-ITS upgrade

- **Upgraded ITS entirely based on CPS**
  - Present detector: 2xHPD/2xDrift-Si/2xSi-strips
  - Future detector: 7-layers with CPS (25-30k chips)

⇒ **1st large tracker (~ 10 m²) using CPS**

- ITS-TDR approved on March 2014

- **New ALICE-ITS requirements**

<table>
<thead>
<tr>
<th></th>
<th>( \sigma_{sp} )</th>
<th>( t_{r.o.} )</th>
<th>Dose</th>
<th>Fluency</th>
<th>( T_{op} )</th>
<th>Power</th>
<th>Active area</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>(&lt; 4 \mu m)</td>
<td>(&lt; 200 \mu s)</td>
<td>150 kRad</td>
<td>(3 \cdot 10^{12} \text{ n}_{eq}/\text{cm}^2)</td>
<td>(30-35^\circ \text{C})</td>
<td>160 mW/cm²</td>
<td>0.15 m²</td>
</tr>
<tr>
<td>ITS-in</td>
<td>(&lt; 5 \mu m)</td>
<td>(&lt; 30 \mu s)</td>
<td>2.7 MRad</td>
<td>(1.7 \cdot 10^{13} \text{ n}_{eq}/\text{cm}^2)</td>
<td>(30^\circ \text{C})</td>
<td>(&lt; 300 \text{ mW/cm}^2)</td>
<td>0.17 m²</td>
</tr>
<tr>
<td>ITS-out</td>
<td>(&lt; 10 \mu m)</td>
<td>(&lt; 30 \mu s)</td>
<td>100 kRad</td>
<td>(1 \cdot 10^{12} \text{ n}_{eq}/\text{cm}^2)</td>
<td>(30^\circ \text{C})</td>
<td>(&lt; 100 \text{ mW/cm}^2)</td>
<td>~ 10 m²</td>
</tr>
</tbody>
</table>

- Different requirements on inner & outer layers calls for different chips designs!

⇒ **0.35 \( \mu m \) CMOS process (STAR-PXL) marginally suited to this r.o. speed & rad. hardness**
CMOS Process Transition: STAR-PXL $\rightarrow$ ALICE-ITS

- PMOS in pixel array not allowed $\Rightarrow$ parasitic q-collection of additional N-well
- Limits choice of readout architecture strategy
- Already demonstrated excellent performances
  - **STAR-PXL**: Mi-28 (AMS 0.35 $\mu$m process)
    $\Rightarrow$ $\varepsilon_{\text{det}} > 99.5\%$, $\sigma_{\text{sp}} < 4\mu$m
  - 1$^{\text{st}}$ CPS detector @ collider experiment

- N-well of PMOS transistors shielded by deep P-well $\Rightarrow$ both types of transistors can be used
- Widens choice of readout architecture strategies
  - **New ALICE-ITS**: 2 sensors R&D in || using TowerJazz CIS 0.18 $\mu$m process (quadru. well)
    - **Synchronous Readout R&D**: proven architecture $\Rightarrow$ safety
    - **Asynchronous Readout R&D**: challenging

Twin well process: 0.6-0.35 $\mu$m

Quadrupole well process (deep P-well): 0.18 $\mu$m
ALICE-ITS: Two Architectures for the pixel chip

**MISTRAL-O**

- **Pixel pitch:** 36x64 μm²
- **Time resolution:** ~ 20 μs
- **W:** 80 mW/cm²
- **Max hit rate:** ~0.8 MHz/cm²
- **Dimension:** 15 x30 mm²
- **Dead area:** 1.5x30 mm²

**Goal:** early available and reliable solution

- **Conservative design based on STAR-PXL**
- **Big pixel ⇒ low power & high speed**
- **Moderate rad. hardness & σsp ~10 μs ⇒ OK**

**ALPIDE**

- **Pixel pitch:** 28x28 μm²
- **Time resolution:** < 5 μs
- **W:** 39 mW/cm²
- **Max hit rate:** ~ 3MHz/cm²
- **Dimension:** 15 x30 mm²
- **Dead area:** 1.1x30 mm²

**Goal:** high performance, accept risks

- **Aggressive design**
- **In-pixel discrimination**
- **Data-driven r.o. (priority encoder)**

**Both chips have same physical & electrical interfaces**

**Base-line solution: ALPIDE for all ITS layers**

Alejandro Pérez Pérez, VERTEX 2017, 14 Sep. 2017
PXL in STAR Inner Detector Upgrades

We track inward from the TPC with graded resolution:

TPC ~1 mm → SSD ~300 μm → IST ~250 μm → PXL ~30 μm

TPC – Time Projection Chamber (main tracking detector in STAR)

HFT – Heavy Flavor Tracker
- SSD – Silicon Strip Detector
  - r = 22 cm
- IST – Inner Silicon Tracker
  - r = 14 cm
- PXL – Pixel Detector
  - r = 2.8, 8 cm

Direct topological reconstruction of Charm – displaced vertices

L. Greiner (CPIX-14)
Technology Perspectives for Performance Improvements

**HV/HR-CMOS sensors:** $d_{\text{dep}} \sim 0.3 \sqrt{\rho_{\text{sub}} U_{\text{bias}}}$
- Extend sensitive volume & improved q-collection
  ⇒ Faster signal & stronger rad. tolerance
- Not bound to CMOS processes using epi-layers
  - Easier access to VDSM (< 100 nm) process
  - Higher in-pixel $\mu$-circuitry density
- Unanswered questions
  - Minimal pixel dimensions ($\sigma_{sp}$) ?
  - Uniformity over large sensitive area & production yield?

**2-tiers chips**
- Signal sensing (front-end) & processing (r.o.) parts distributed over two interconnected tiers (AC coupling)
- Smart sensor ⇒ 1 r.o. pixel addressing N pixel-front-ends
  ⇒ Reduce density of interconnections
- Can combine 2 diff. CMOS processes: front-end/r.o.
- **Benefits:** small pixels ⇒ resolution, speed, data-compression and robustness
- **Challenges:** interconnection technology (reliability & cost)

P. Rymaszewski et al, arXiv:1601.00459

Alejandro Pérez Pérez, VERTEX 2017, 14 Sep. 2017
Sensor technologies

- Technologies proposed so far

- Fine pixel (x20 more pixels)
- Standard pixel (x20 time slice in 1 train)
- Standard pixel (Bunch ID in 1 train)

FPCCD
- ISIS
- FAPS
- Chronopixel
- SCCCD
- MAPS
- SOI
- CPCCCD
- DEPFET

Bunch Train

Bunch Spacing

20170502

LC Vertex Detector Workshop 2017
DEPFET Active Pixels

- FET gate
- clear gate
- amplifier
- p+ source
- n+ clear
- p+ drain
- deep n-doping 'internal gate'
- depleted n-Si bulk
- deep p-well
- p+ back contact

- DEPMOS device
- Gate
- Source
- Drain
- Clear-gate
- Clear
- I\textsubscript{bias}
- \text{I2U converter}
- \text{V}_{\text{out}}
- \text{R}_{f}
- \text{R}_{s}
- \text{V}_{\text{SS}}
- \text{V}_{\text{Drain}}
DEPFET all-silicon module for Belle II

DCDB (Drain Current Digitizer)
- Analog front-end
- Amplification and digitization of DEPFET signals.
- 256 input channels
- 8-bit ADC per channel
- 92 ns sampling time
- UMC 180 nm
- Rad hard design

SwitcherB - Row Control
- AMS/IBM HVCMOS 180 nm
- Size 3.6 x 1.5 mm²
- Gate and Clear signal
- 32x2 channels
- Fast HV ramp for Clear
- Rad. Hard proved (36 Mrad)

DHP (Data Handling Processor)
- First data compression
- TSMC 65 nm
- Size 4.0 x 3.2 mm²
- Stores raw data and pedestals
- Common mode and pedestal correction
- Data reduction (zero suppression)
- Timing and trigger control
- Rad. Hard proved (100 Mrad)

Key to low mass vertex detectors

- MCMs w/ highest possible integration!
- Thin sensor area
- EOS for r/o ASICs
- Thin (perforated) frame w/ steering ASICs
Full Size Modules

- 768x250 DEPFET Pixels
- 50x75 $\mu$m$^2$ pixel pitch
- 75 $\mu$m thickness

1. Power up. Voltage sanity check
2. ASIC Sanity check. JTAG boundary scan
3. Digital test pattern, delay scans
4. Switcher control signals
5. Raw data readout
6. Pedestal distribution, noise
7. Response on radioactive sources
CMOS Pixel Sensors for the ILD-VXD (2/2)

- From the STAR-PXL to the ILC-VXD:

<table>
<thead>
<tr>
<th>Detector</th>
<th>$\sigma_{sp}$</th>
<th>$t_{int}$</th>
<th>Dose (30°C)</th>
<th>Fluence (30°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>STAR-PXL</td>
<td>$\gtrsim 3.5 \mu m$</td>
<td>190 $\mu s$</td>
<td>150 kRad</td>
<td>$3 \times 10^{12} n_{eq}/cm^2$</td>
</tr>
<tr>
<td>ILD-VXD/In</td>
<td>$&lt; 3 \mu m$</td>
<td>50/10 $\mu s$</td>
<td>$&lt; 100$ kRad</td>
<td>$\lesssim 10^{11} n_{eq}/cm^2$</td>
</tr>
<tr>
<td>ILD-VXD/Out</td>
<td>$\lesssim 4 \mu m$</td>
<td>100 $\mu s$</td>
<td>$&lt; 10$ kRad</td>
<td>$\lesssim 10^{10} n_{eq}/cm^2$</td>
</tr>
</tbody>
</table>

- Final ”500 GeV” CPS prototypes: fab. in Winter 2011/12 (0.35 $\mu m$ process for economic reasons)

- **MIMOSA-30**: inner layer prototype with 2-sided read-out
  - one side: 256 pixels ($16 \times 16 \mu m^2$)
  - other side: 64 pixels ($16 \times 64 \mu m^2$)

- **MIMOSA-31**: outer layer prototype
  - 48 col. of 64 pixels ($35 \times 35 \mu m^2$)
  - ended with 4-bit ADC
Potential of MIMOSIS

- Extension of MIMOSIS to an ILC vertex detector
  - Reoptimise trade-off between requirements (relax rad. tolerance & hit rate capability)
  - Shrink pixel dimensions to minimum
  - Reshuffle read-out structure
  - Translate to smaller feature size: TowerJazz 110/180 nm, 150 or 130 nm technologies

- Sensor target performances:
  - Spatial resolution $\lesssim 4 \mu m$
  - Time resolution $\sim 2\text{–}4 \mu s$
  - Non-sensitive side-band width reduced to $\sim 1 \text{ mm}$

- MIMOSIS prototyping (1 MPW, 3 ER until 2020) allows for ILC prototyping
Sensor Integration in Ultra-Light devices

PLUME collaboration (Bristol, DESY, IPHC)

Plume 01 prototype (fabricated in 2012)
- 2x6 Mi26 sensors on 2 mm thick foam SiC (0.6% $X_0$)
- Air cooling
- Validated in beam @ CERN (2011)
- New test-beam @ DESY in April 2016

Plume 02 prototype: 6 ladders for 2016
- Reduced material budget: → 0.35/0.42 % $X_0$ (Al/Cu flex PCB)

Application outside ILC
- Beam-bkg measurement @ Belle II
- 2 Plume 02 ladders will be installed inside Belle II inner volume in 2017
- FOOT
**Design concepts: PLUME**

- **PLUME initial choices**
  - Double-sided
  - Thinned sensors (50 μm)
    - Start with a CPS ➔ might change if other options available
    - MIMOSA-26: single point resolution 3 μm, integration time 115 μs
  - Spacer
    - Silicon Carbide foam, 2 mm thickness, few % density
  - Air cooling
    - Sensor to sit on top
  - Sensitive length 125 mm ➔ 6 MIMOSA-26 per side
  - Connexions with wire bonding
Design Concepts: assembly

- **Step 1**
  - Aligning & gluing sensors to FPCs
  - **Automatic** placement machine

- **Step 2**
  - Wire bonding on individual FPCs

- **2 Modules**

- **Step 3**
  - Gluing 2 modules simultaneously on both sides of a SiC foam
  - **Manually** with a dedicated jigs
  - **1 Ladder**

Module assembly robot

Ladder assembly jigs
Outputs of PLUME-2

- **Aluminium FPC more fragile**
  - Quality of metal traces OK in sensor area
  - BUT SMD connector mounting badly reliable
    - All 4 AI modules have unstable connexion
  - Possible fix:
    - use bonding to connect cable to outside
    - Probable impact on ladder assembly → still not yet done

- **Narrow 4% SiC foam is brittle**
  - Need extra-car / transportation
    - Two proto-ladders had the part sticking out for support broken

- **Tests with Cu version**
  - Only in-lab characterization so far
    - No suspicious behaviour
  - Metrology survey / deformation
    - In preparation at Bristol/Oxford
  - Beam tests @ DESY 2017/18
  - Test in a collider (SuperKEKB) in 2018
PLUME outside ILC

- **Beam-induced background @ SuperKEKB**
  - BEAST II will measure up to $1 \times 10^{34} \, \text{cm}^2/\text{s}$
    - dedicated setup PRIOR the final Belle II full vertex detector
    - Feb-Jun 2018 = data taking
  - 2 PLUME-2 ladders at various radius and angles
    - Assess hit rate online
    - Exploit 2-sided info to recognize bkgrnd types

- **FOOT (INFN) project**
  - Measures nuclear fragmentation of interest for hadrontherapy
  - Need tracker for low momentum (<300 MeV) fragments
    - Requirement $\sigma_{p/p} \sim 3\%$
  - Tracker in 2 parts
    - 1st station = individual sensors
    - 2nd station = 8x8 cm$^2$
      - 4 new PLUME-type ladders (exploit MIMOSA-28)
    - Design with LNF (E. Spiriti)
ILC Tracking system expected performances: \( p_T \) resolution

- **Results from full simulation single muon particle gun**
  - Empirical parametrization
    \[
    \sigma(1/p_T) = a \oplus b/p_T \sin \theta \text{ GeV}^{-1}
    \]
  - **SiD**
    - \( a = (2 - 4) \times 10^{-5}, \ b = (2 - 5) \times 10^{-3} \)
    - Better @ high \( p_T \)
    - Robustness in high density track environment
  - **ILD**
    - \( a = \sim 2 \times 10^{-5}, \ b \sim 1 \times 10^{-3} \)
    - Better @ low \( p_T \)
    - dE/dx capabilities (TPC)
ILC Tracking system expected performances: Flavour tagging

- ILD example
- Full simulation
- Multi-variable tagging algorithm (BDT)
  - LCFIplus
- Continuous improvements
I-LGAD: Test beam results

Beetle ROC
Fan in DC
Fan in AC
Strip LGAD
Strip I-LGAD

I-LGAD
(Room temp. 400 Volts)

Standard Strip
(Room temp. 200 Volts)

Cluster Charge (arb. Units)

Gain ~ 250/80 ~ 38/13 ~ 3